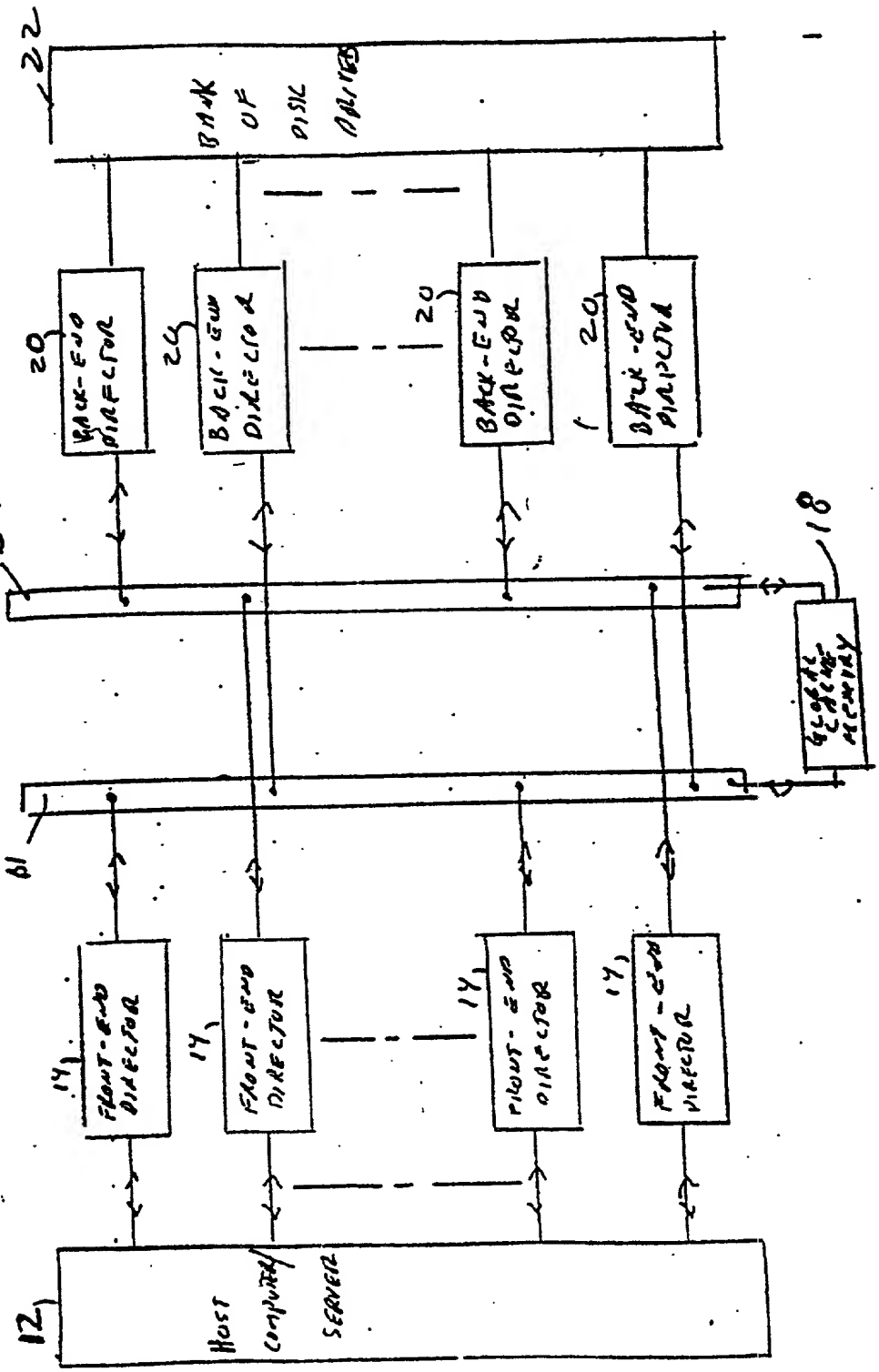


FIG. 1
PRIOR ART

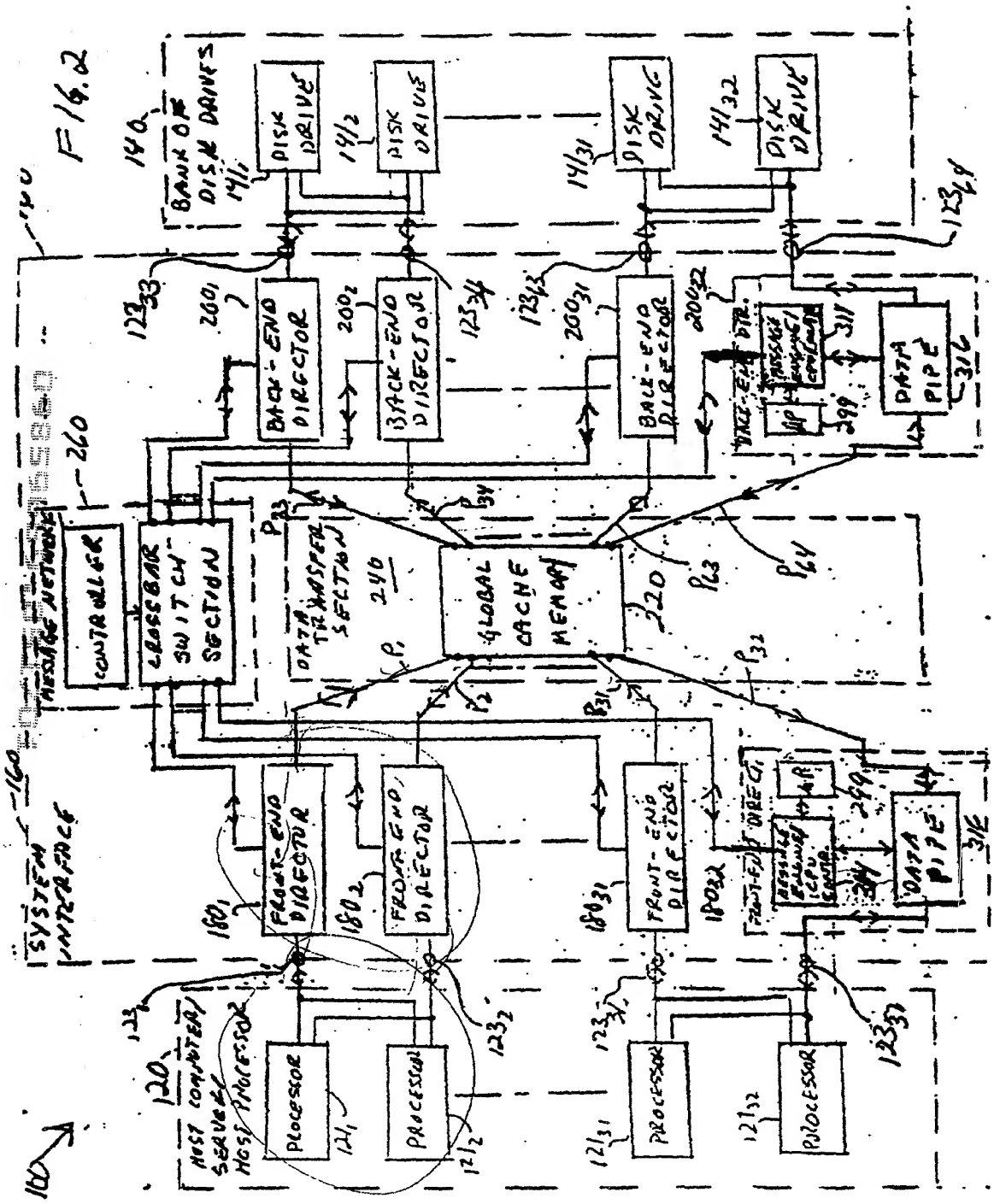


FIG. 2
100
120
HOST COMPUTER/ SERVER/ HOST PROCESSOR
121
PROCESSOR
123
140
BANK OF DISK DRIVES
141
DISK DRIVE
160
SYSTEM INTERFACE
180
FRONT-END DIRECTOR
200
BACK-END DIRECTOR
240
DATA TRANSFER SECTION
220
GLOBAL CACHE MEMORY
260
MESSAGE NETWORK
CONTROLLER
CROSSBAR SWITCH SECTION
312
DATA PIPE

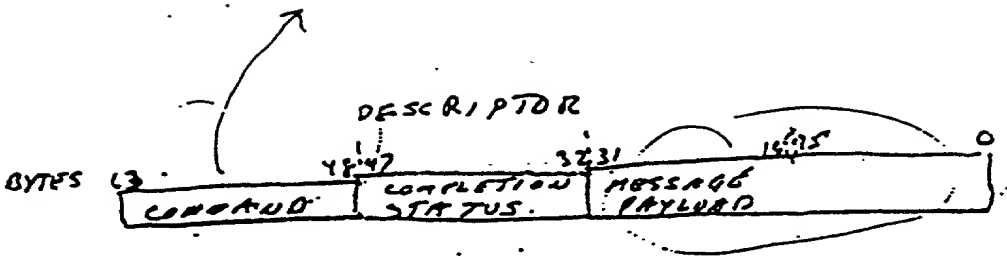

DESCRIPTOR
BYTES
63
48:47
32:31
16:15
0
COMMAND
COMPLETION STATUS
MESSAGE PAYLOAD

FIG 2A

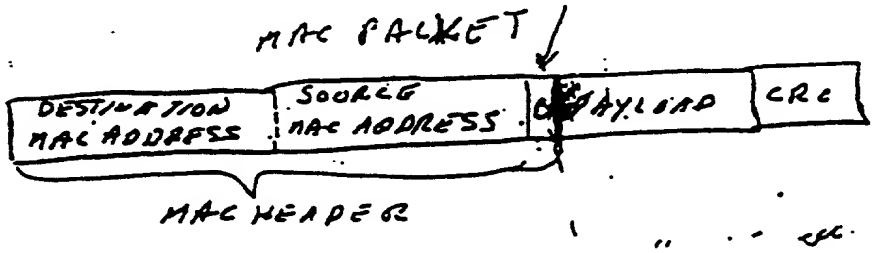

MAC PACKET
DESTINATION MAC ADDRESS
SOURCE MAC ADDRESS
PAYLOAD
CRC
MAC HEADER

FIG 2B

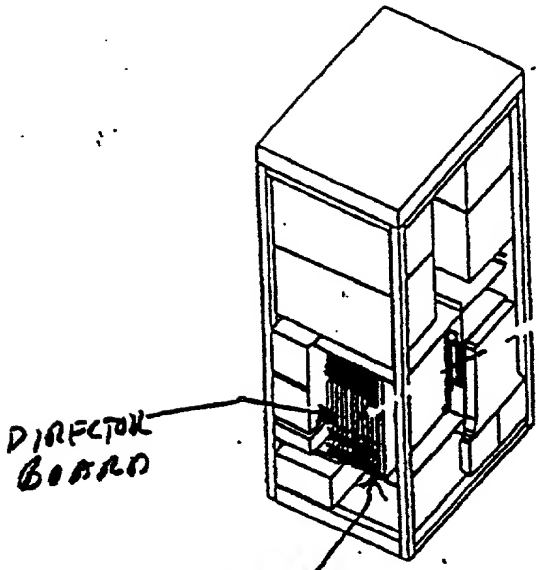
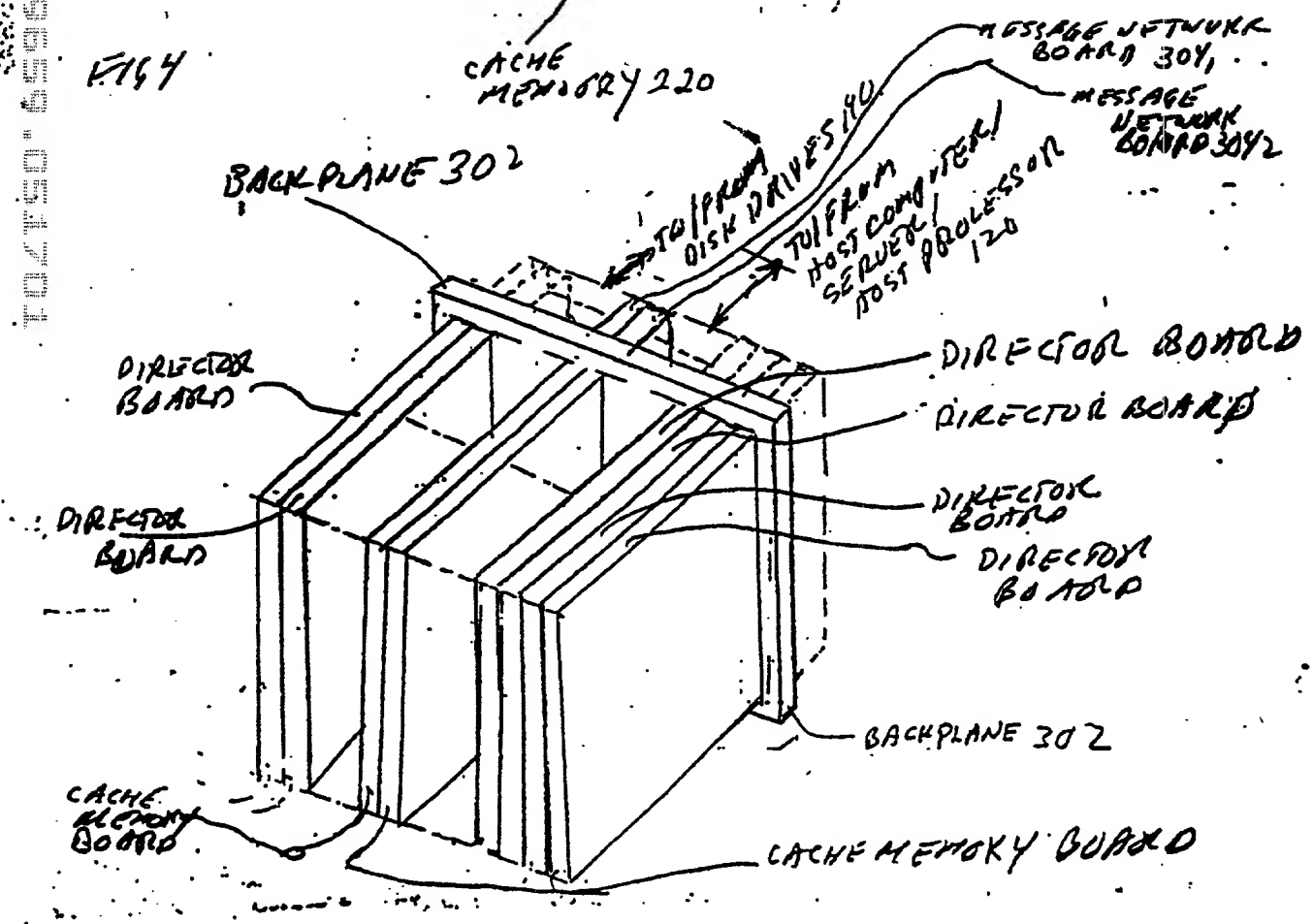

DIRECTOR
BOARD
CACHE
MEMORY 220

FIG. 3

FIG 4


MESSAGE NETWORK
BOARD 304,
MESSAGE
NETWORK
BOARD 304,2
BACKPLANE 302
TO/FROM
DISK DRIVES 140
TO/FROM
HOST COMPUTER/
HOST PROCESSOR
120
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR
BOARD
DIRECTOR
BOARD
DIRECTOR
BOARD
DIRECTOR
BOARD
BACKPLANE 302
CACHE
MEMORY
BOARD
CACHE MEMORY BOARD

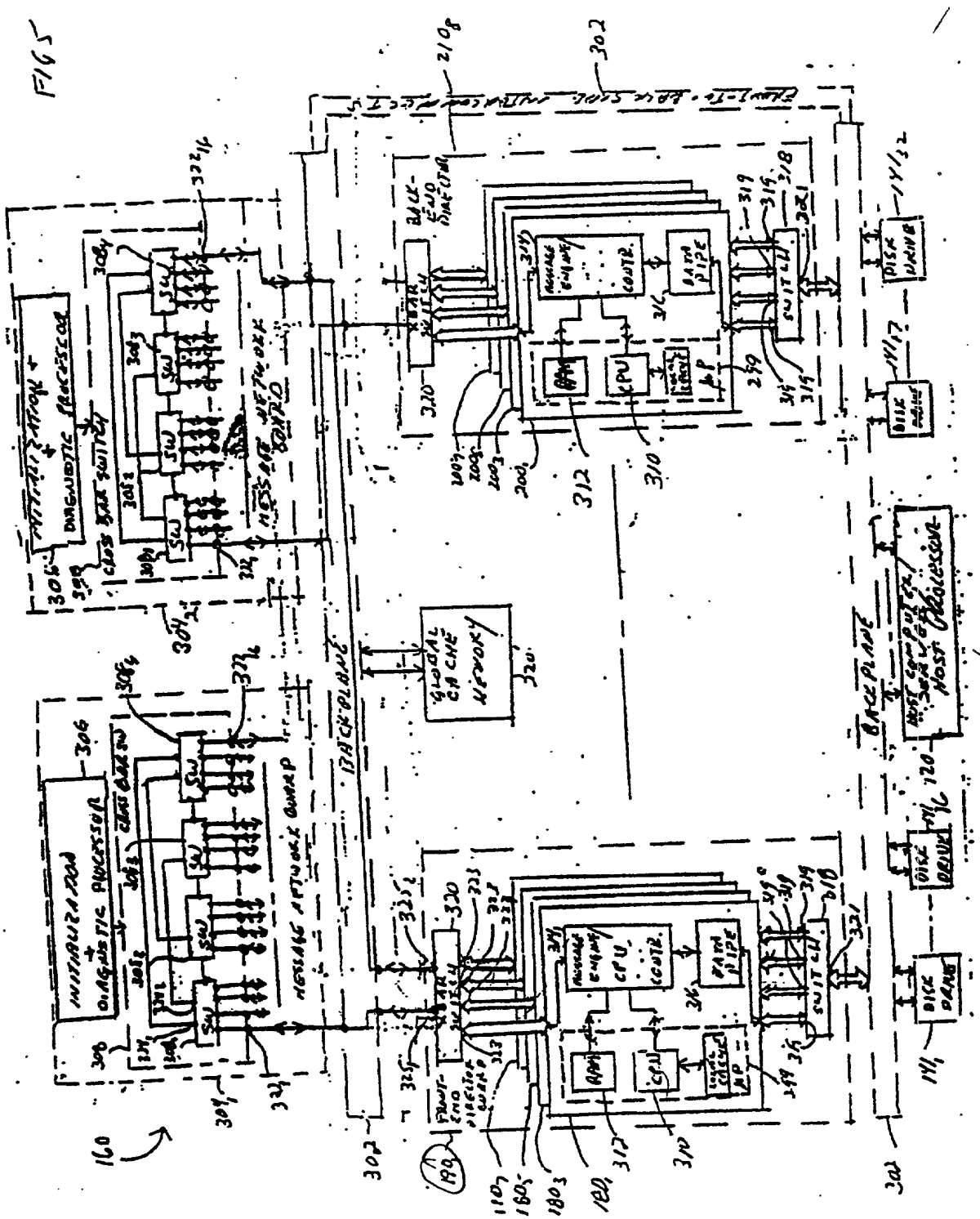
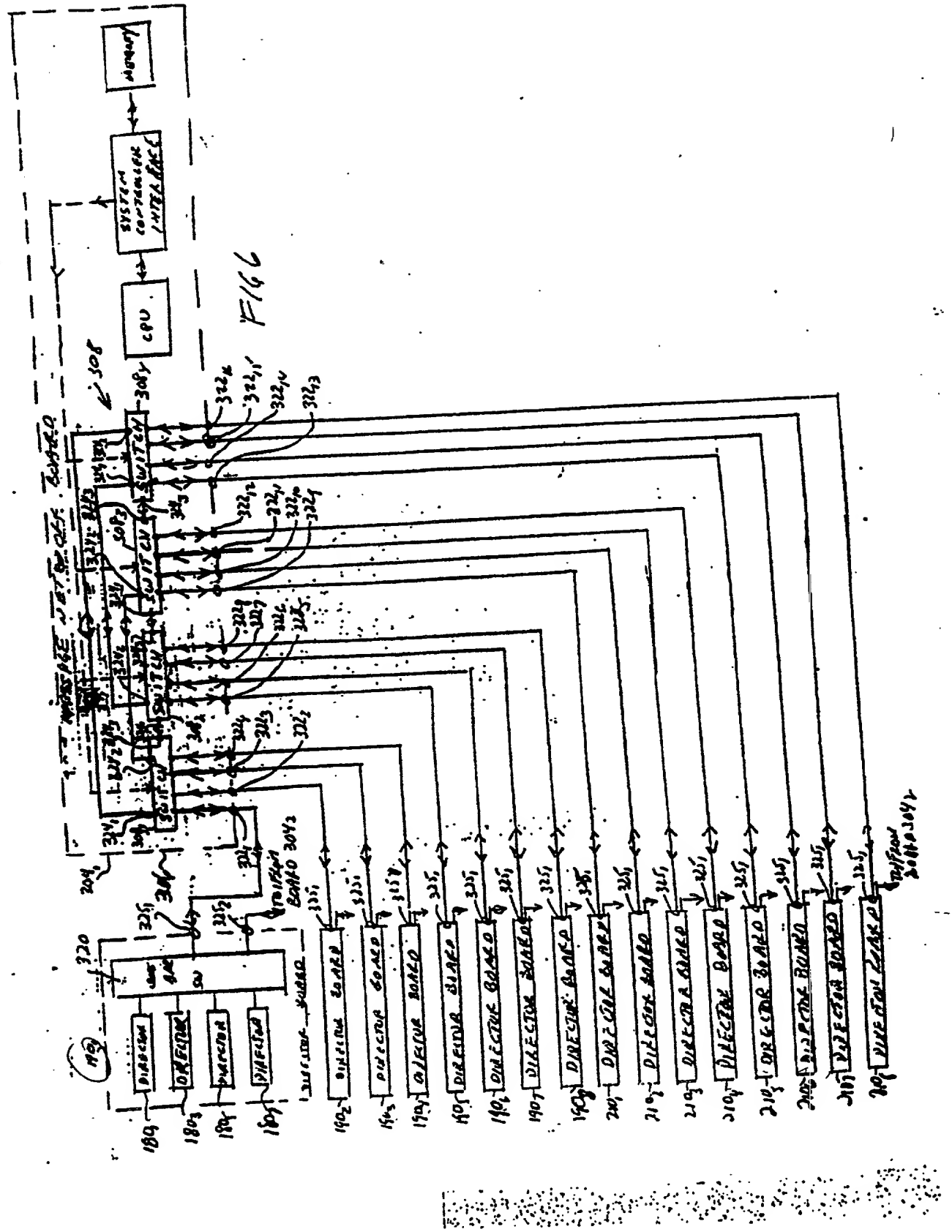


FIG 5
160
302
310
312
320
GLOBAL CACHE MEMORY
DISK DRIVE
DISK DRIVE
DISK DRIVE
DISK DRIVE


CPU
SYSTEM CONTROLLER INTERFACE
MEMORY
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD

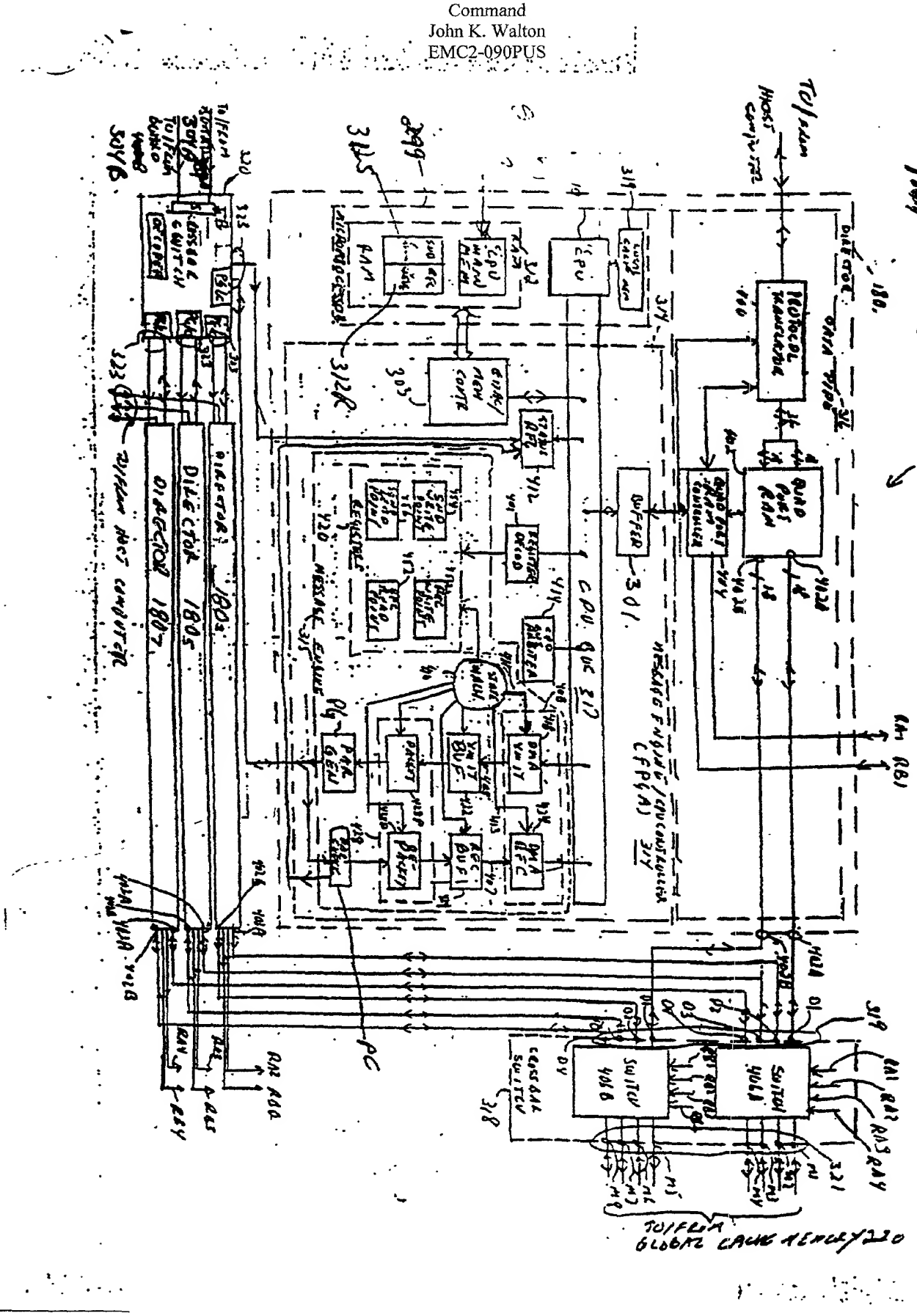


FIG 7
DIRECTOR 1805
DIRECTOR 1807
DIRECTOR 1803
CPU
SWITCH
SWITCH
GLOBAL CACHE MEMORY 230
MESSAGE MANAGER (CMM) 317
CPU BUS 311
PC

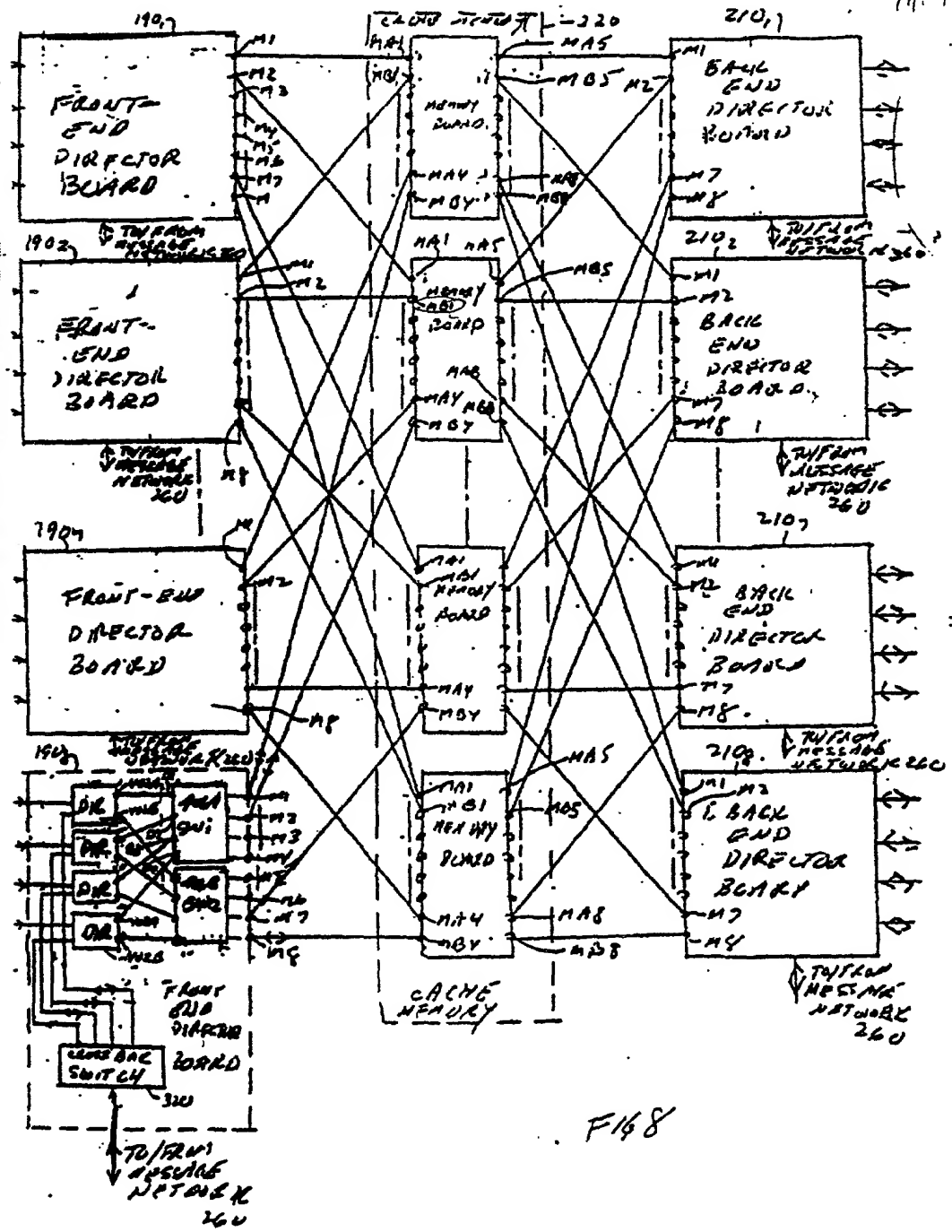

FRONT-END DIRECTOR BOARD
BACK END DIRECTOR BOARD
MEMORY BOARD
CACHE MEMORY
SWITCH
TO/FROM MESSAGE NETWORK 260

FIG 8

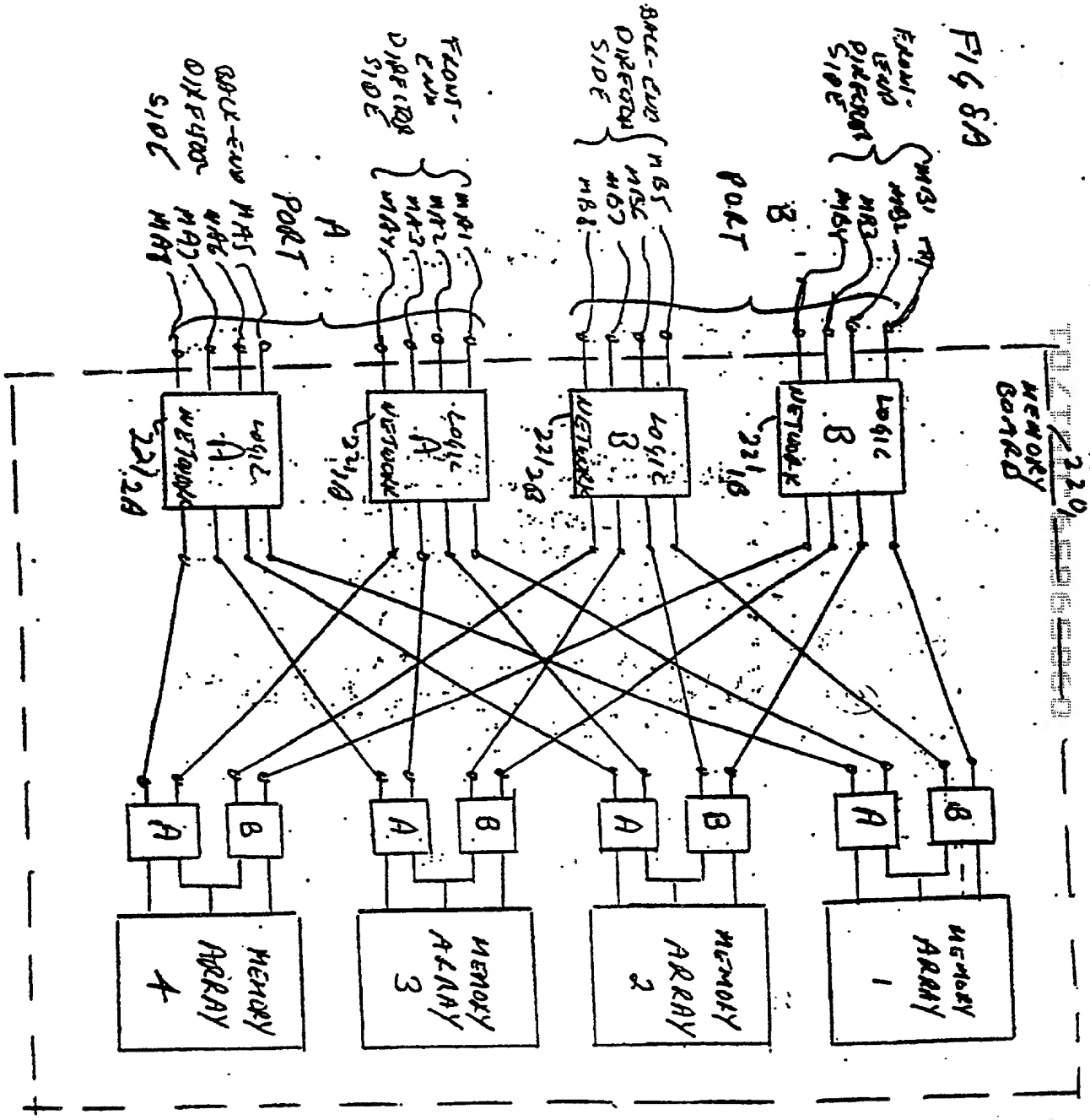


FIG 8A
MEMORY BOARD
220
B PORT
A PORT
FRONT-END DIRECTOR SIDE
BACK-END DIRECTOR SIDE
LOGIC B NETWORK
LOGIC A NETWORK
MEMORY ARRAY 1
MEMORY ARRAY 2
MEMORY ARRAY 3
MEMORY ARRAY 4

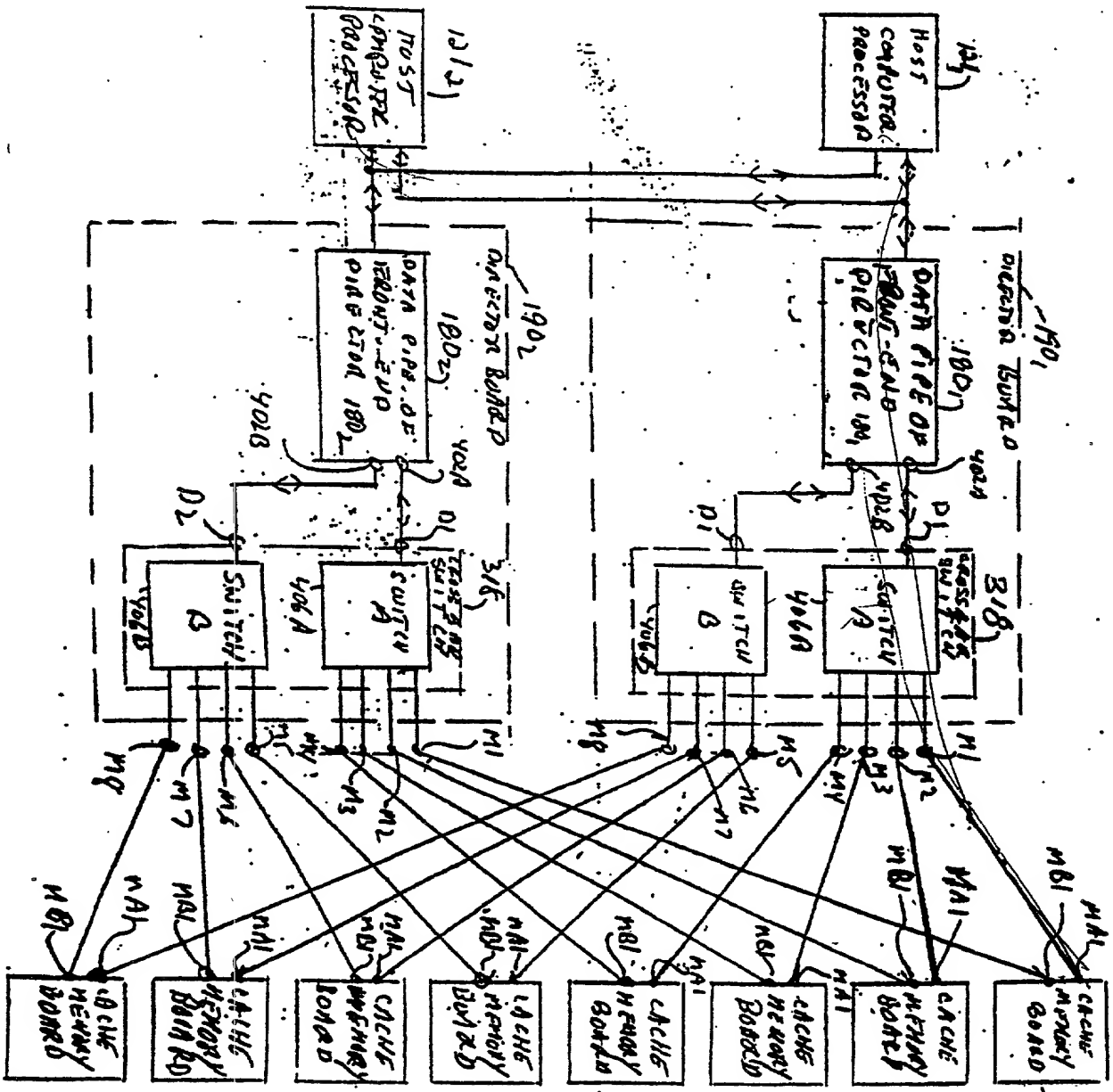
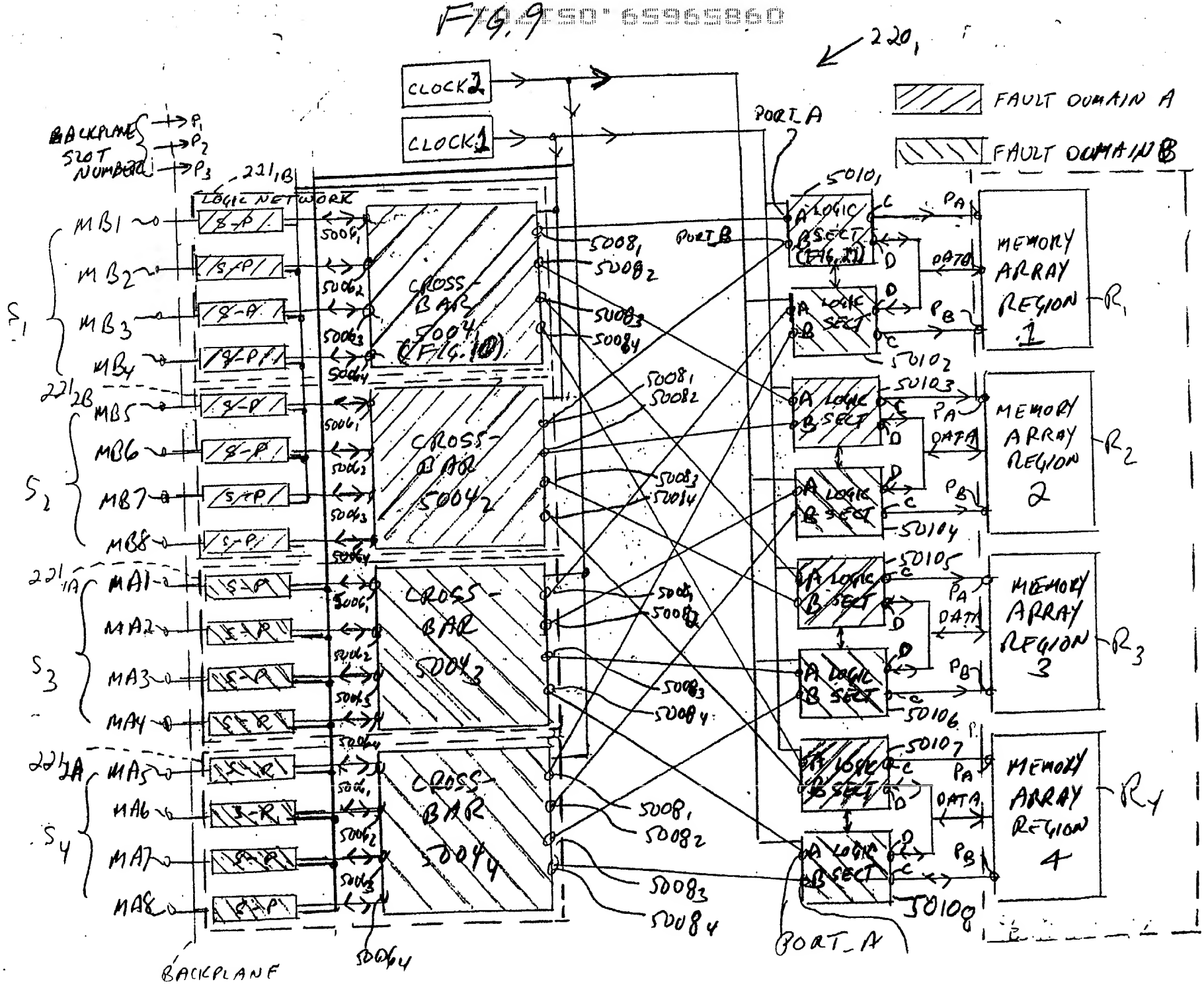

HOST COMPUTER PROCESSOR
DATA PIPE OF DIRECTOR
SWITCH A
SWITCH B
CACHE MEMORY BOARD
CACHE MEMORY BOARD
CACHE MEMORY BOARD
CACHE MEMORY BOARD
CACHE MEMORY BOARD
CACHE MEMORY BOARD
CACHE MEMORY BOARD
CACHE MEMORY BOARD

FIG 8B

FIG. 9


220₁
CLOCK 2
CLOCK 1
FAULT DOMAIN A
FAULT DOMAIN B
PORT_A
PORT_B
BACKPLANE SLOT NUMBER
P1
P2
P3
221₁B
LOGIC NETWORK
MB1
MB2
MB3
MB4
MB5
MB6
MB7
MB8
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
S1
S2
S3
S4
221₂B
221₁A
221₂A
CROSS BAR 5004
(FIG. 10)
CROSS BAR 5004₂
CROSS BAR 5004₃
CROSS BAR 5004₄
5006₁
5006₂
5006₃
5006₄
5008₁
5008₂
5008₃
5008₄
5010₁
5010₂
5010₃
5010₄
5010₅
5010₆
5010₇
5010₈
LOGIC A SECT (FIG. 11)
LOGIC B SECT
PA
PB
DATA
MEMORY ARRAY REGION 1
MEMORY ARRAY REGION 2
MEMORY ARRAY REGION 3
MEMORY ARRAY REGION 4
R1
R2
R3
R4
BACKPLANE
PORT_A
PORT_B

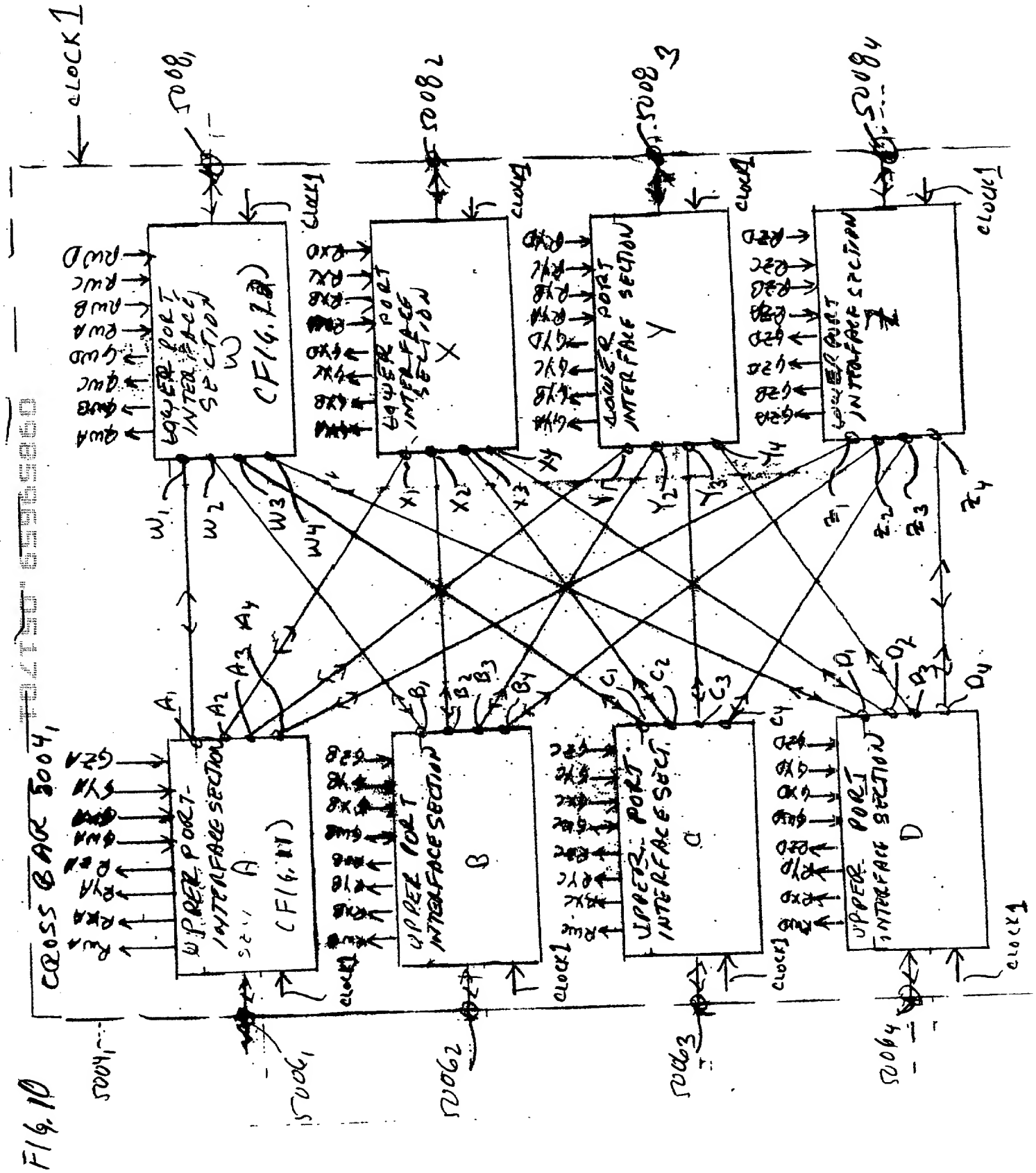

CROSS BAR SOC 4
CLOCK 1
SOC 1
SOC 2
SOC 3
SOC 4
LOWER PORT INTERFACE SECTION
UPPER PORT INTERFACE SECTION
A
B
C
D
W
X
Y
Z

FIG. 10

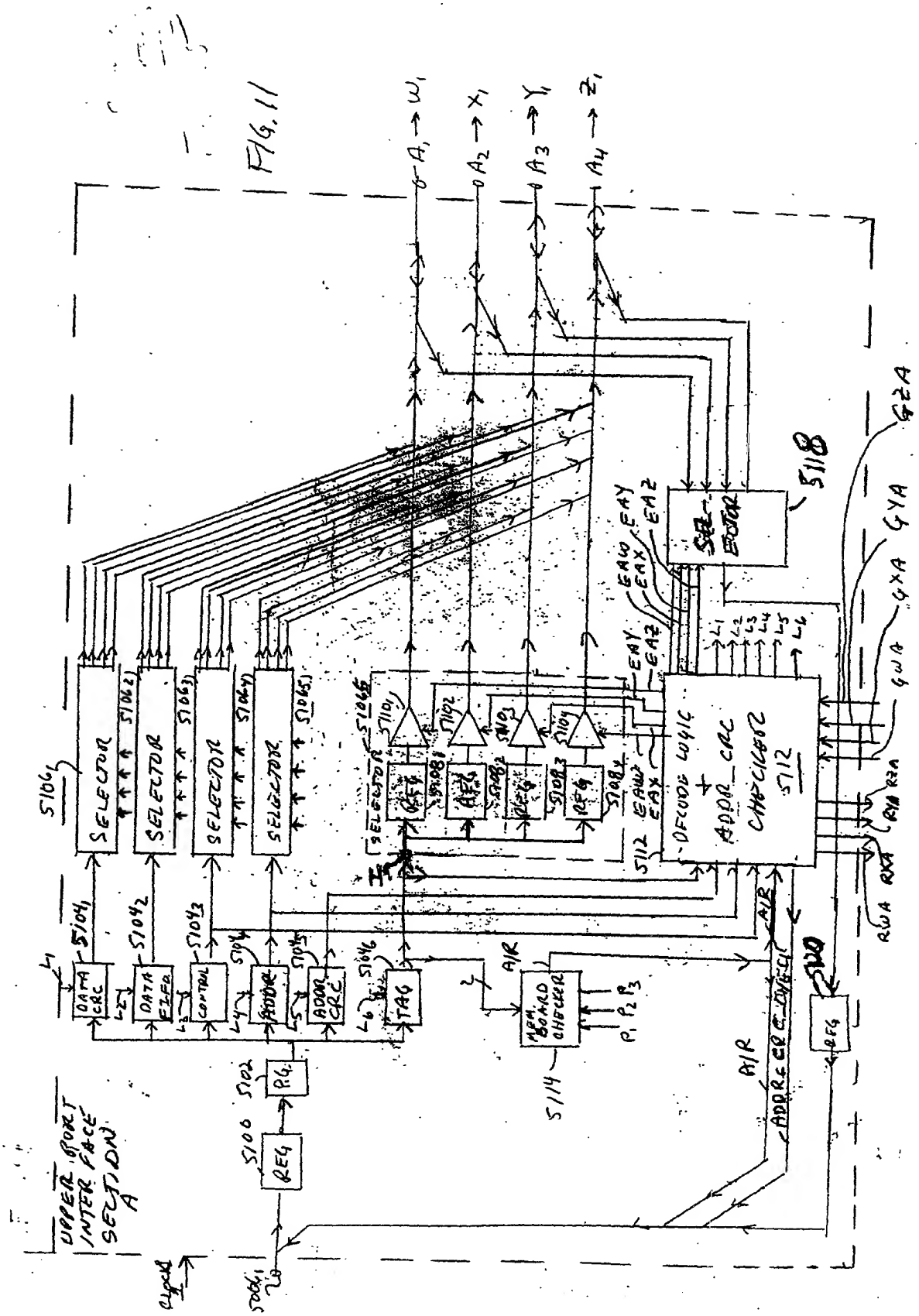
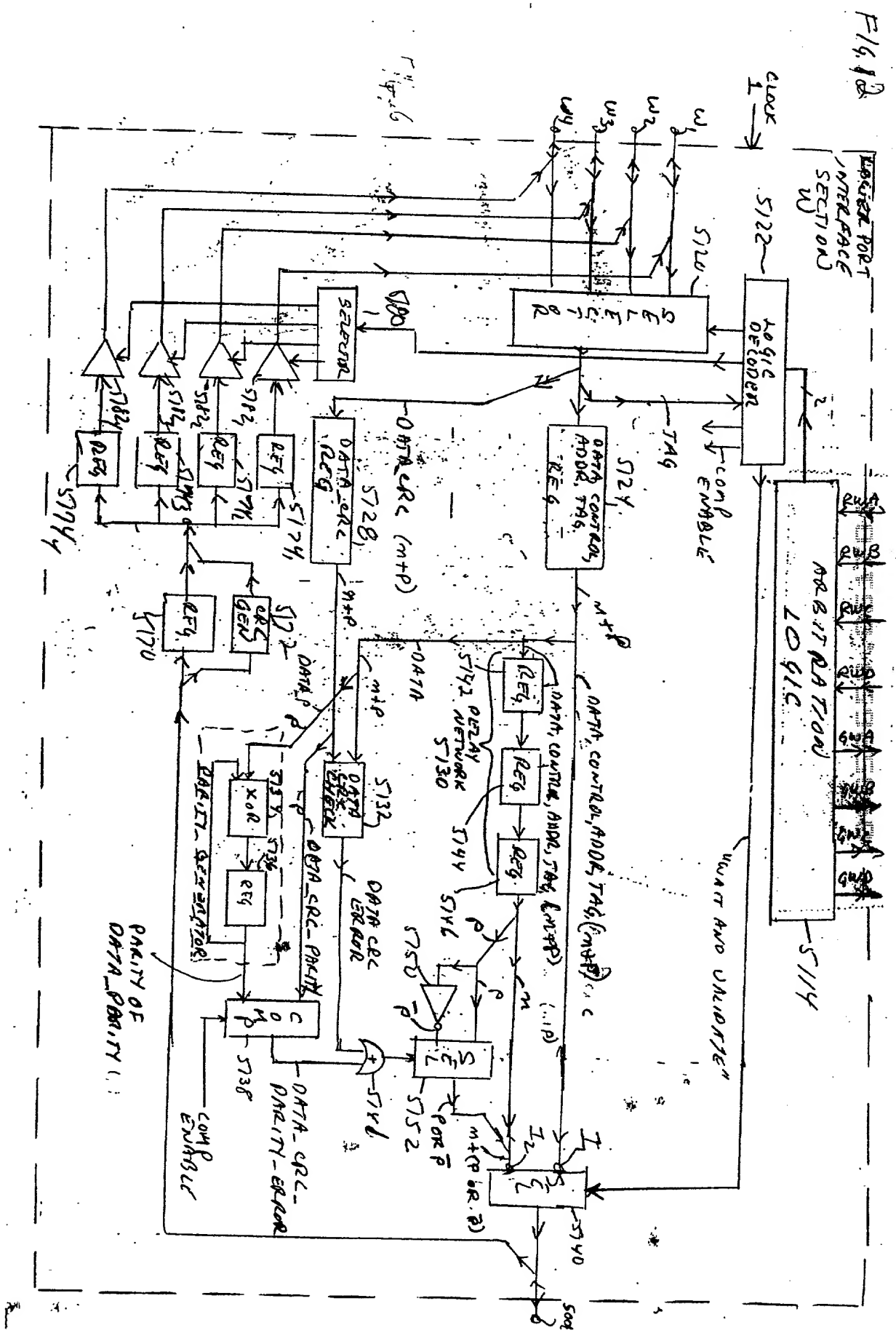


FIG. 11
UPPER FRONT END INTERFACE SECTION
SELECTOR
DATA CRC
DATA EZFEA
CONTROL
ADDR
ADDR CRC
TAG
REG
MEM BOARD CHECKER
DECODE LOGIC
ADDR CRC CHECKER
ADDR & CD CHECKER
A1 → W1
A2 → X1
A3 → Y1
A4 → Z1
GZA
GYA
GXA
GWA
RWA
RXA
RYA
RZA
EAW
EAX
EAY
EAZ
A/R
S100
S102
S104
S106
S108
S110
S112
S114
S116
S118

Data Storage System Having No-Operation Command
John K. Walton
EMC2-090PUS



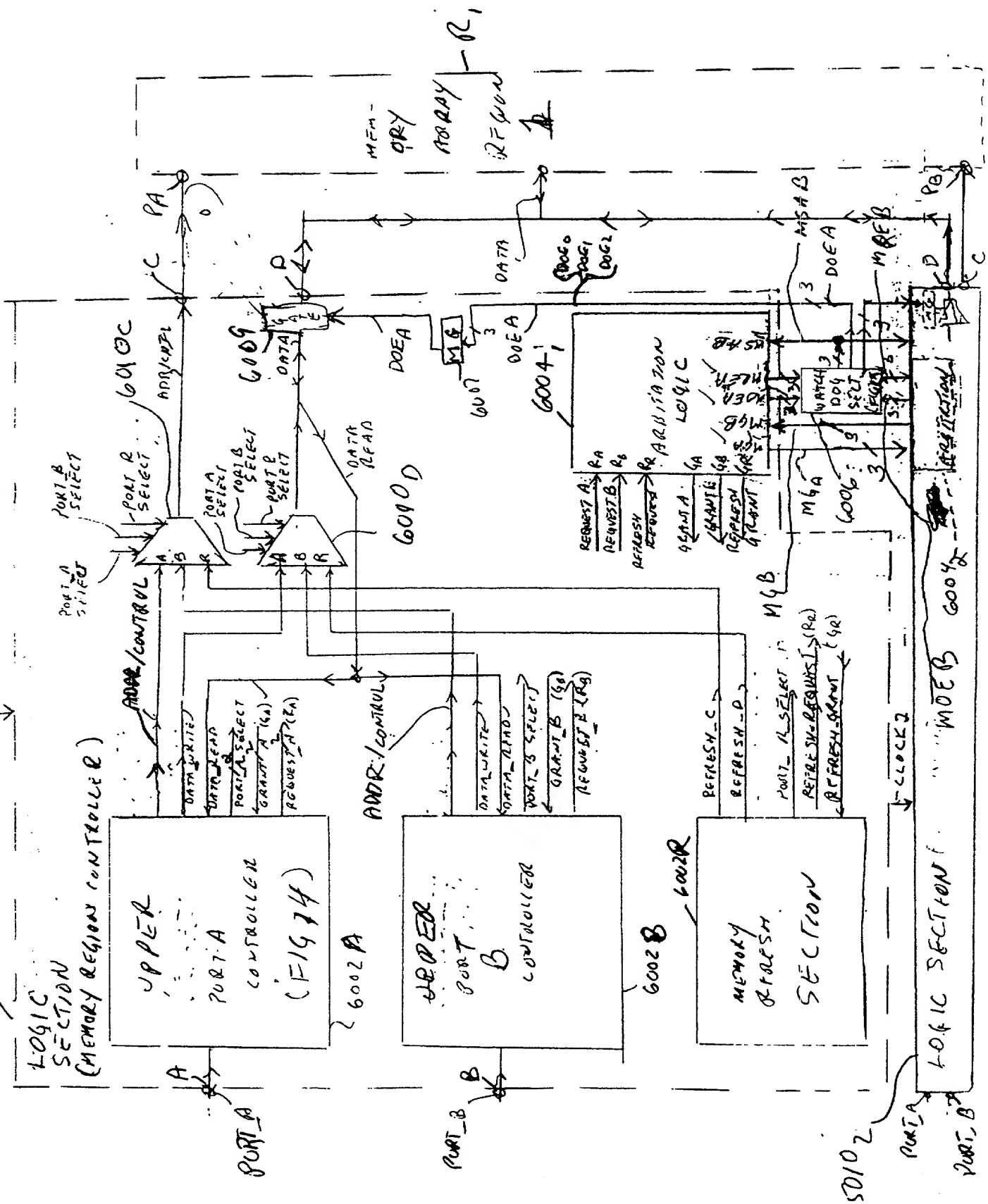

LOGIC SECTION (MEMORY REGION CONTROLLER)
5010
UPPER PORT A CONTROLLER (HIGH)
6002A
UPPER PORT B CONTROLLER
6002B
MEMORY REFRESH SECTION
6002R
ADDR/CONTROL
DATA WRITE
DATA READ
PORT_A_SELECT
GRANT_A (GA)
REQUEST_A (RA)
PORT_B_SELECT
GRANT_B (GB)
REQUEST_B (RB)
REFRESH_C
REFRESH_D
PORT_A
PORT_B
MEM-ORY ARRAY
REGION 1
6004
ARBITRATION LOGIC
WATCH DOG SELECT
CLOCK2
5010
LOGIC SECTION
PORT_A
PORT_B

FIG. 1

Data Storage System Having No-Operation Command
John K. Walton
EMC2-090PUS

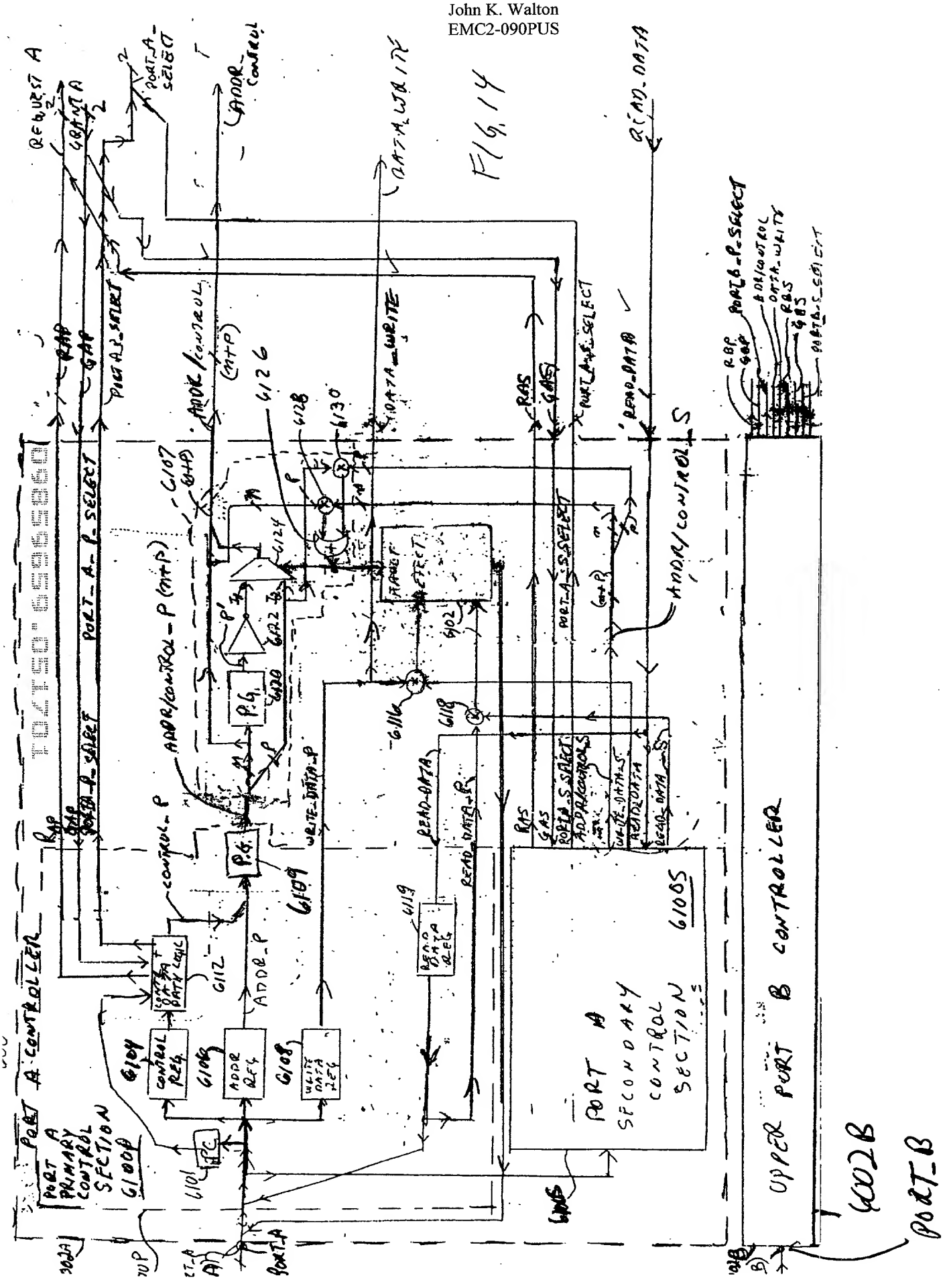
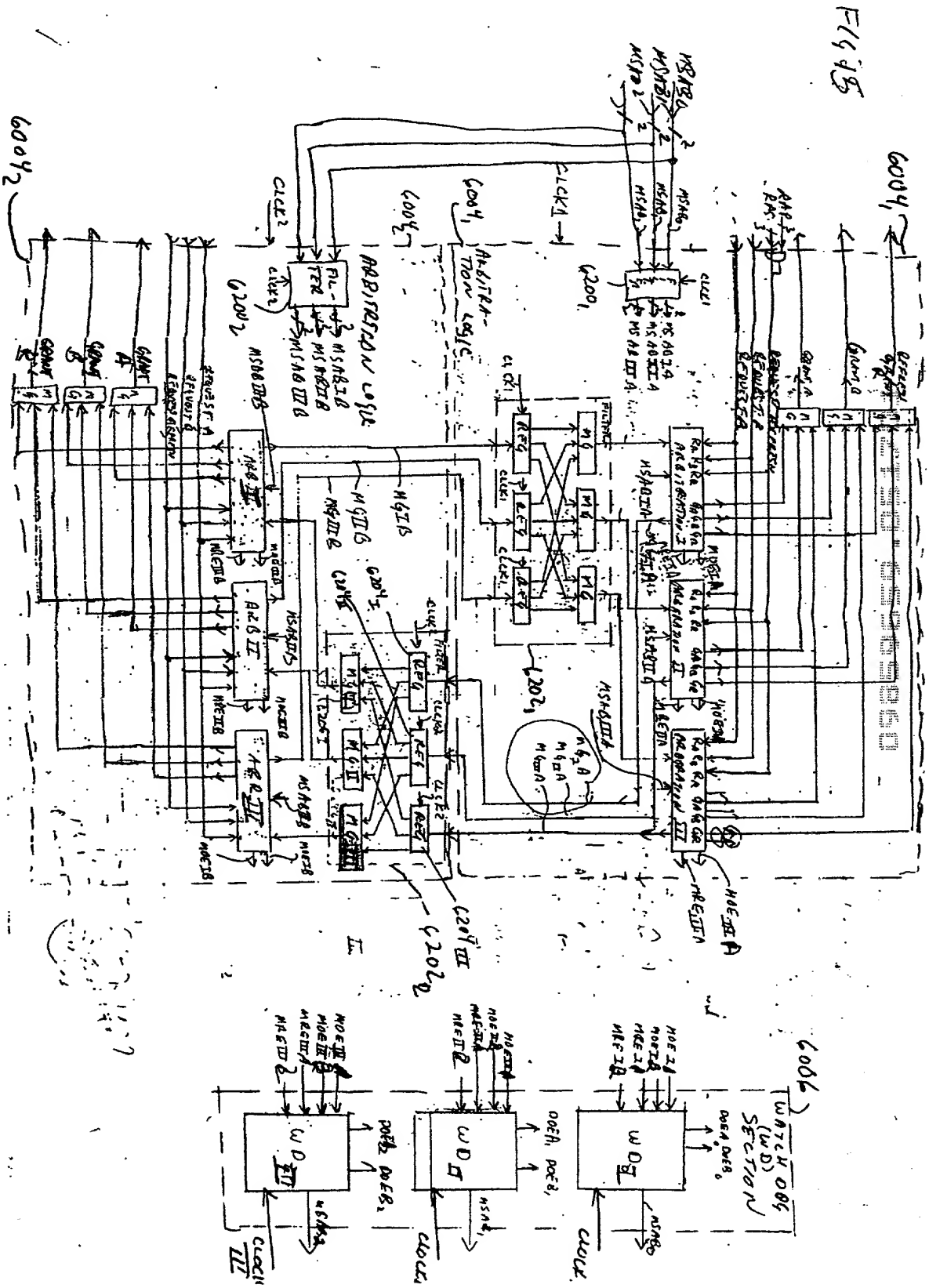


FIG. 14



Data Storage System Having No-Operation Command
John K. Walton
EMC2-090BUS

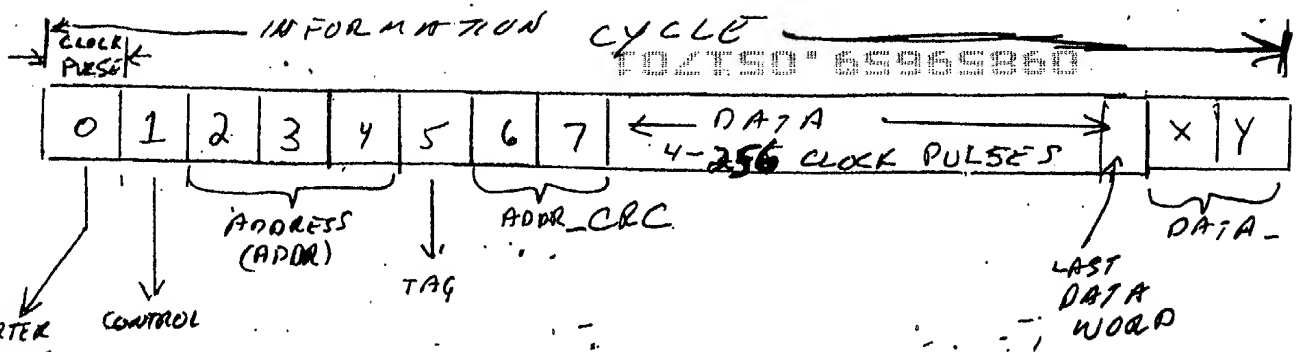


FIG. 16

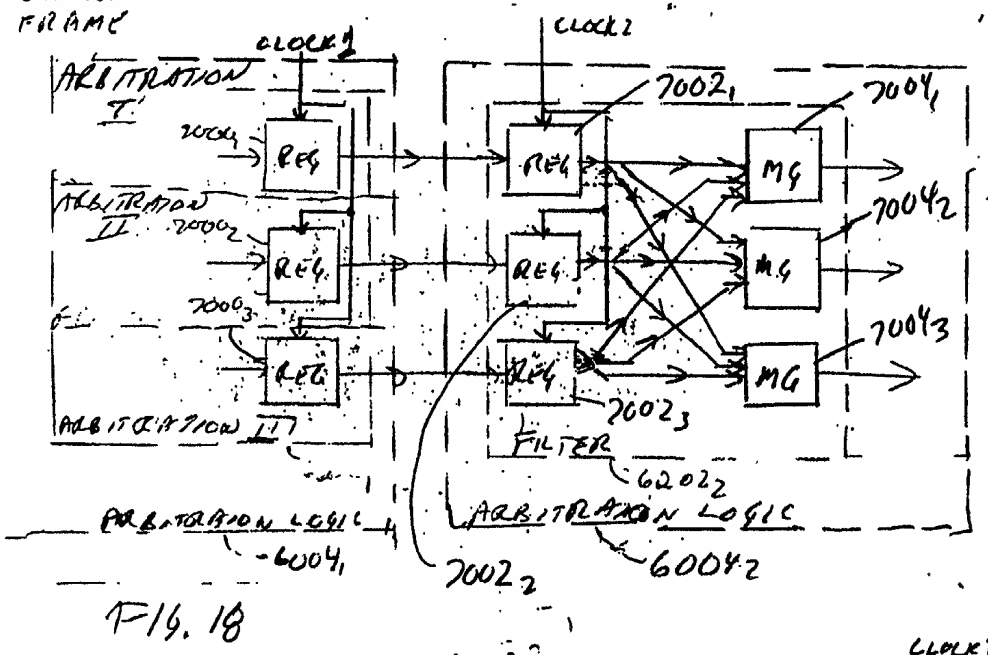


FIG. 18

FIG. 17

MG INPUTS	MG OUTPUT	MG OUTPUT	MG OUTPUT
0 0 0	0	0	0
0 0 1	0	0	0
0 1 0	0	0	0
0 1 1	1	1	1
1 0 0	0	0	0
1 0 1	1	1	1
1 1 0	1	1	1
1 1 1	1	1	1

FIG. 19

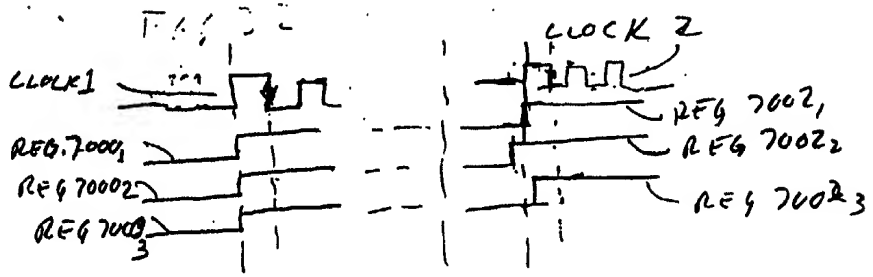
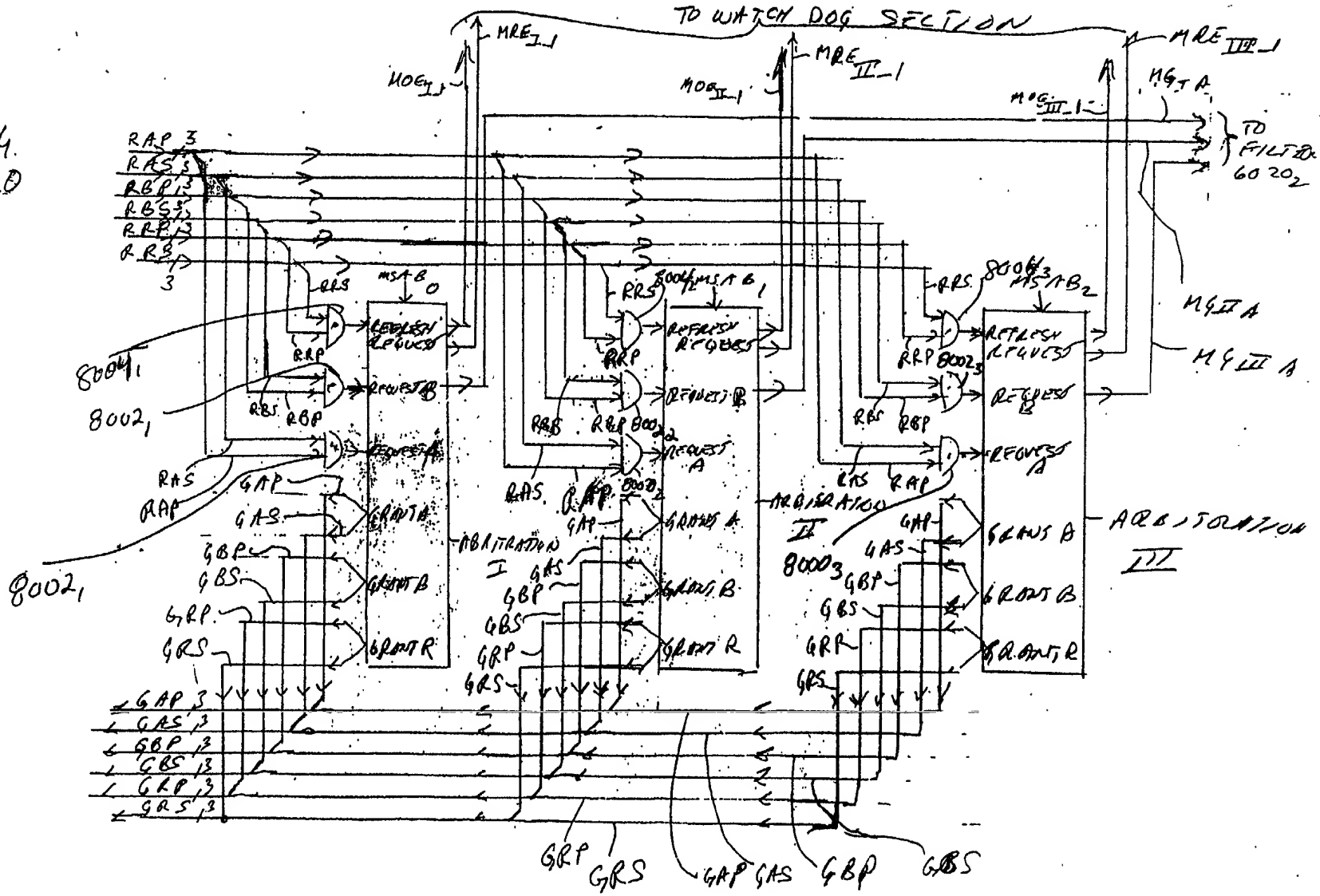


FIG. 20


TO WATCH DOG SECTION
MRE I-1
MRE II-1
MRE III-1
MOG I-1
MOG II-1
MOG III-1
MG I A
MG II A
MG III A
TO FILTER 60 20
RAP 3
RAS 3
RBP 3
RBS 3
RRP 3
RRS 3
RRS
RRP
RBS
RBP
MSAB 0
MSAB 1
MSAB 2
REFRESH REQUEST
REQUEST B
REQUEST A
RAS
RAP
GAP
GAS
GBP
GBS
GRP
GRS
GRANT A
GRANT B
GRANT R
ARBITRATION I
ARBITRATION II
ARBITRATION III
8002 1
8002 2
8002 3
GAP 3
GAS 3
GBP 3
GBS 3
GRP 3
GRS 3